

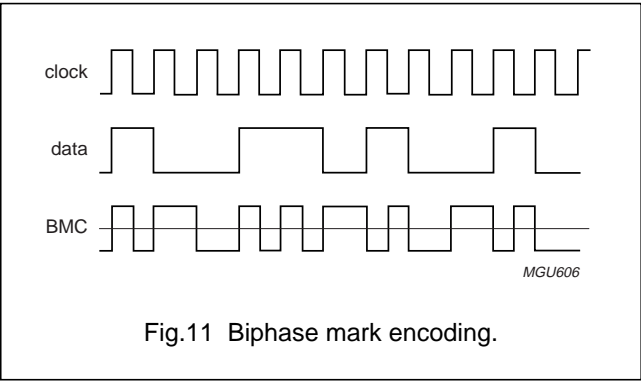
Stereo audio codec with SPDIF interface

UDA1355H

9 SPDIF SIGNAL FORMAT

9.1 SPDIF channel encoding

The digital signal is coded using Biphas Mark Code (BMC), which is a kind of phase modulation. In this scheme, a logic 1 in the data corresponds to two zero-crossings in the coded signal, and a logic 0 to one zero-crossing. An example of the encoding is given in Fig.11.

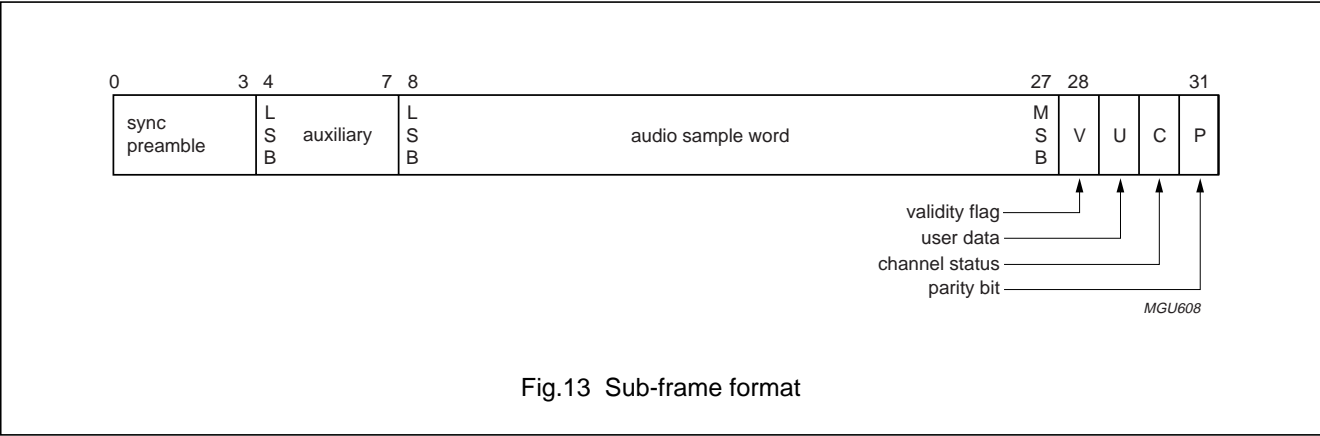
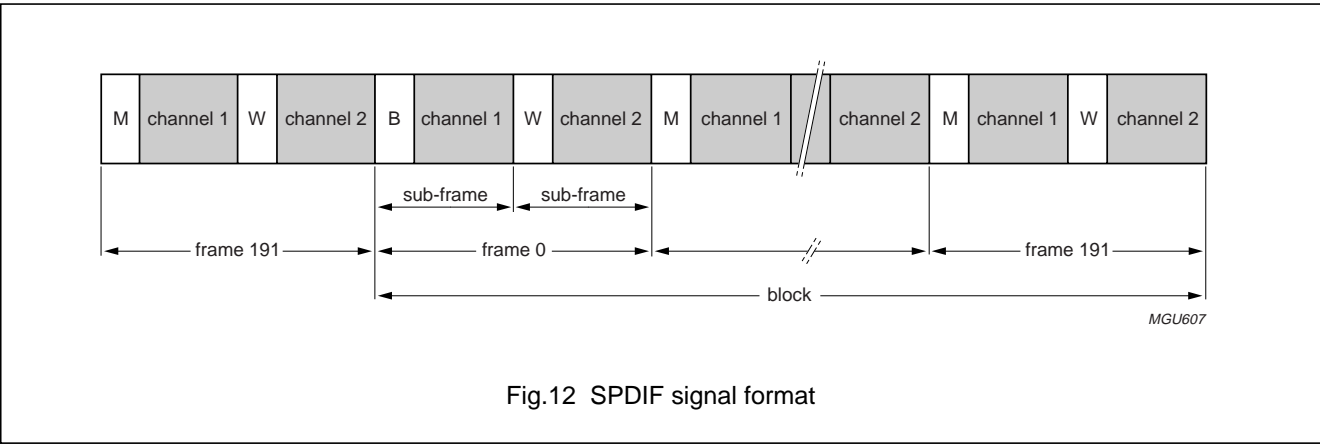


9.2 SPDIF hierarchical layers

The SPDIF signal format is shown in Fig.12. A PCM signal is transmitted in sequential blocks. Each block consists of 192 frames. Each frame contains two sub-frames, one for each channel. Each subframe is preceded by a preamble. There are three types of preambles: B, M and W. Preambles can be spotted easily in an SPDIF bitstream because these sequences never occur in the channel parts of a valid SPDIF bitstream.

The sub-frame format is represented by Fig.13. A sub-frame contains a single audio sample word which may be 24 bits wide, a validity bit which indicates whether the sample is valid, a bit containing user data, a bit indicating the channel status and a parity bit for this sub-frame.

The data bits 31 to 4 in each sub-frame are encoded using a BMC scheme. The sync preamble contains a violation of the BMC scheme and can be detected. Table 15 indicates the values of the preambles.



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**Table 15** Preambles

PRECEDING STATE	CHANNEL CODING	
	0	1
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

**9.3 Timing characteristics****9.3.1 FREQUENCY REQUIREMENTS**

The SPDIF specification IEC 60958 supports three levels of clock accuracy:

- Level I high accuracy: Tolerance of transmitting sampling frequency shall be within  $50 \times 10^{-6}$
- Level II, normal accuracy: All receivers should receive a signal of  $1000 \times 10^{-6}$  of nominal sampling frequency
- Level III, variable pitch shifted clock mode: A deviation of 12.5% of the nominal sampling frequency is possible.

The UDA1355H inputs support level I, II, and III as specified by the IEC 60958 standard.

**9.3.2 RISE AND FALL TIMES**

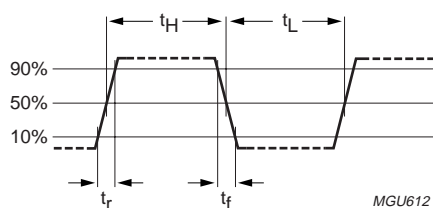
Rise and fall times (see Fig.14) are defined as:

$$\text{Rise time} = \frac{t_r}{t_L + t_H} \times 100\%$$

$$\text{Fall time} = \frac{t_f}{t_L + t_H} \times 100\%$$

Rise and fall times should be in the range:

- 0% to 20% when the data bit is a logic 1
- 0% to 10% when the data bits are two succeeding logic 0.

**Fig.14** Rise, fall time and duty cycle.**9.3.3 DUTY CYCLE**

The duty cycle (see Fig.14) is defined as:

$$\text{Duty cycle} = \frac{t_H}{t_L + t_H} \times 100\%$$

The duty cycle should be in the range:

- 40% to 60% when the data bit is a logic 1
- 45% to 55% when the data bits are two succeeding logic 0.

**10 L3-BUS DESCRIPTION**

The exchange of data and control information between the microcontroller and the UDA1355H is accomplished through a serial hardware L3-bus interface comprising the following pins:

- MP0: mode line with signal L3MODE
- MP1: clock line with signal L3CLOCK
- MP2: data line with signal L3DATA.

The exchange of bytes in L3-bus mode is LSB first.

The L3-bus format has two modes of operation:

- Address mode
- Data transfer mode.

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 bits (see Fig.15). The data transfer mode is characterized by L3MODE being HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically two types of data transfers can be defined:

- Write action: data transfer to the device
- Read action: data transfer from the device.

**10.1 Device addressing**

The device address consists of one byte with:

- Data Operating Mode (DOM) bits 0 and 1 representing the type of data transfer (see Table 16)
- Address bits 2 to 7 representing a 6-bit device address.